What is claimed is:

1. A memory device, comprising:

a matrix of memory cells; and

an arrangement of write lines electrically isolated from the memory cells and configured to write data to the memory cells, wherein each write line of the arrangement is electrically coupled to a reverse current limiting device.

2. The memory device of claim 1, wherein the reverse current limiting device includes a diode.

3. The memory device of claim 2, wherein the diode is a Schottky barrier diode.

4. The memory device of claim 2, wherein the diode is a thin film diode.

5. The memory device of claim 1, wherein the matrix of memory cells is one of a plurality of matrices of memory cells, each matrix occupying a different layer of the memory device, and wherein each layer of the memory device includes an arrangement of write lines that are electrically isolated from the memory cells of that layer, each write line of the arrangement being electrically coupled to a reverse current limiting device.

6. The memory device of claim 5, wherein each write line is addressable via a bridge switch and a ladder switch.

7. The memory device of claim 6, wherein the bridge switch includes a write transistor electrically coupled to plural write lines of a layer.

8. The memory device of claim 7, wherein the ladder switch includes a write transistor electrically coupled to a write line of plural layers.

9. The memory device of claim 7, wherein the bridge switch is controlled via a logic subsystem including diode logic gates.

10. The memory device of claim 9, wherein the diode logic gates include thin film diodes.

11. The memory device of claim 6, wherein the ladder switch includes a write transistor electrically coupled to a write line of plural layers.

12. The memory device of claim 11, wherein the ladder switch is controlled via a logic subsystem including diode logic gates.

13. The memory device of claim 12, wherein the diode logic gates include thin film diodes.

14. The memory device of claim 6, wherein the reverse current limiting device electrically coupled to a write line is electrically interposed between the bridge switch and the ladder switch configured to address that write line.

15. The memory device of claim 5, further comprising, for each layer of the memory device, an arrangement of read lines electrically coupled to the memory cells of that layer, and an arrangement of read/write lines electrically coupled to the memory cells of that layer.

16. The memory device of claim 1, wherein the matrix of memory cells include semiconductor memory cells.

17. The memory device of claim 1, wherein the arrangement of write lines includes a plurality of substantially coplanar parallel write lines.

18. A memory device, comprising:

a first matrix of memory cells occupying a first layer of the memory device;

a first arrangement of write lines electrically isolated from the first matrix of memory cells and configured to write data to the first matrix of memory cells, wherein each write line of the first arrangement of write lines is electrically coupled to a thin film diode configured to limit reverse current;

at least a second matrix of memory cells occupying a second layer of the memory device; and

a second arrangement of write lines electrically isolated from the second matrix of memory cells and configured to write data to the second matrix of memory cells, wherein each write line of the second arrangement of write lines is electrically coupled to a thin film diode configured to limit reverse current.

19. The memory device of claim 18, wherein the write lines of the first arrangement share a bridge switch with other write lines of the first arrangement, and the write lines of the second arrangement share a bridge switch with other write lines of the second arrangement.

20. The memory device of claim 19, wherein each write line of the first arrangement shares a ladder switch with a write line of the second arrangement.

21. The memory device of claim 20, wherein, for each write line, the thin film diode electrically coupled to that write line is electrically interposed between the bridge switch and the ladder switch shared by that write line.

22. The memory device of claim 18, wherein each write line of the first arrangement shares a ladder switch with a write line of the second arrangement.

23. The memory device of claim 18 further comprising a first arrangement of read lines and a first arrangement of read/write lines.

24. The memory device of claim 23, wherein the read lines and the read/write lines intersect at a plurality of cross-points, and wherein a memory cell is electrically coupled to a read line and a read/write line at each cross-point.

25. A method of fabricating a memory device with reduced semiconductor area; the method comprising:

providing at least a first layer of memory cells;

disposing an arrangement of write lines about each layer of memory cells, wherein each write line is electrically isolated from the memory cells; and

electrically incorporating a thin film diode configured to limit reverse current into each write line.

26. The method of claim 25, further comprising providing a write addressing system including ladder and bridge transistors.

27. The method of claim 26, further comprising providing a logic subsystem including diode logic gates, wherein the logic subsystem is configured to selectively activate the ladder and bridge transistors to allow current to pass through selected write lines.

28. A memory device, comprising:

a matrix of data storing means; and

an arrangement of data writing means electrically isolated from the data storing means and configured to write data to the data storing means, wherein each data writing means of the arrangement is electrically coupled to a reverse current limiting means.

29. A memory device, comprising:

a matrix of memory cells;

an arrangement of write lines configured to write data to the memory cells; and

a write addressing system including a plurality of write transistors, the write transistors collectively configured to provide write selectivity to each write line by conditionally allowing current to pass through selected write lines, wherein the write addressing system includes a logic subsystem that includes a plurality of diode logic gates, wherein the logic subsystem is configured to selectively activate the write transistors to allow current to pass through the selected write lines.

30. The memory device of claim 29, wherein the diode logic gates include thin film diodes.

31. The memory device of claim 29, wherein the arrangement of write lines are electrically isolated from the matrix of memory cells.